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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Ret
1	☑	☐	US 20020031012 A1	20020314	26	Method for manufacturing non-volatile memory cell	365/185.26		
2	☑	☐	US 20010015911 A1	20010823	26	Method for operating non-volatile memory cells	365/185.26		
3	☑	☐	US 6353556 B1	20020305	23	Method for operating non-volatile memory cells	365/185.26	365/185.29; 365/185.33	
4	☑	☐	US 6249459 B1	20010619	23	Circuit and method for equalizing erase rate of	365/185.26	365/185.22; 365/185.29	
5	☑	☐	US 6219281 B1	20010417	23	System and method for erasing non-volatile memory	365/185.29	365/185.19; 365/185.33	
6	☑	☐	US 6198662 B1	20010306	23	Circuit and method for pre-erasing/erasing flash	365/185.29	365/185.33; 365/218	
7	☑	☐	US 6166962 A	20001226	23	Circuit and method for conditioning flash memory	365/185.3	365/185.24; 365/185.29	

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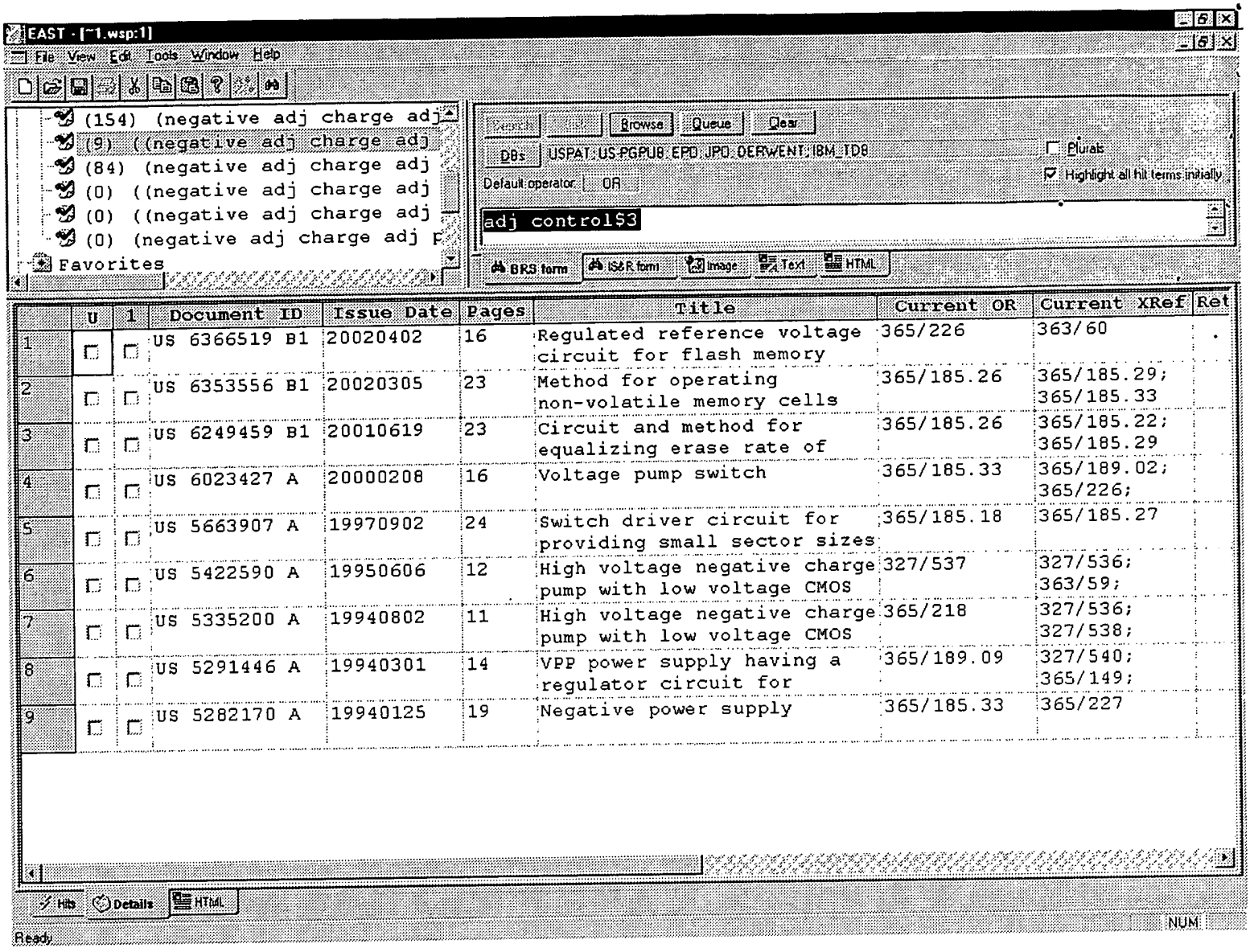

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Ret
1	☐	☐	US 6366519 B1	20020402	16	Regulated reference voltage circuit for flash memory	365/226	363/60	
2	☐	☐	US 6353556 B1	20020305	23	Method for operating non-volatile memory cells	365/185.26	365/185.29; 365/185.33	
3	☐	☐	US 6249459 B1	20010619	23	Circuit and method for equalizing erase rate of	365/185.26	365/185.22; 365/185.29	
4	☐	☐	US 6023427 A	20000208	16	Voltage pump switch	365/185.33	365/189.02; 365/226;	
5	☐	☐	US 5663907 A	19970902	24	Switch driver circuit for providing small sector sizes	365/185.18	365/185.27	
6	☐	☐	US 5422590 A	19950606	12	High voltage negative charge pump with low voltage CMOS	327/537	327/536; 363/59;	
7	☐	☐	US 5335200 A	19940802	11	High voltage negative charge pump with low voltage CMOS	365/218	327/536; 327/538;	
8	☐	☐	US 5291446 A	19940301	14	VPP power supply having a regulator circuit for	365/189.09	327/540; 365/149;	
9	☐	☐	US 5282170 A	19940125	19	Negative power supply	365/185.33	365/227	

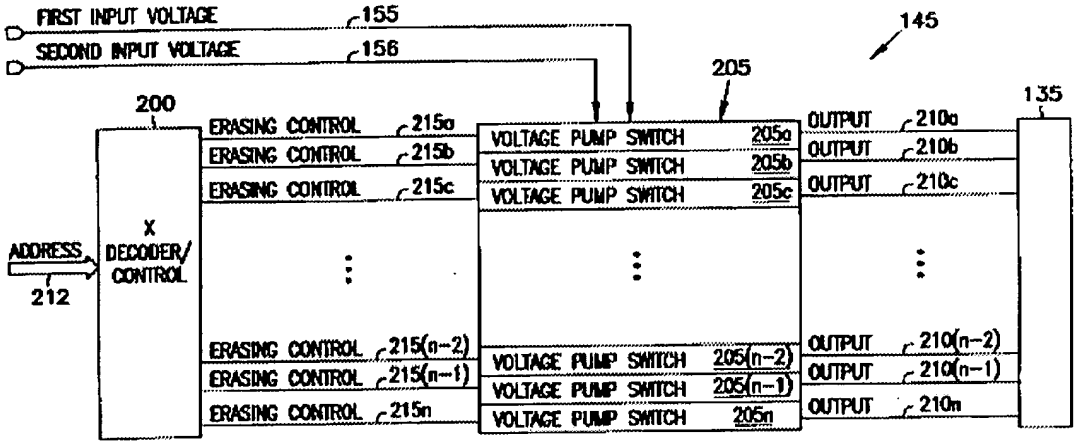

FIG. 2

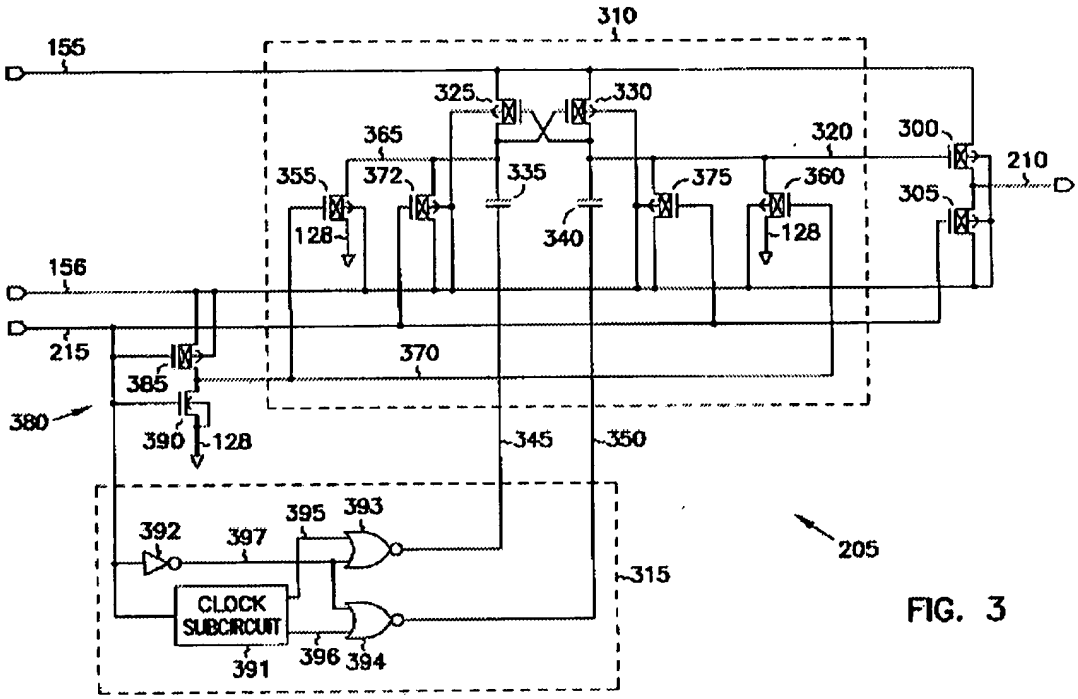

FIG. 3

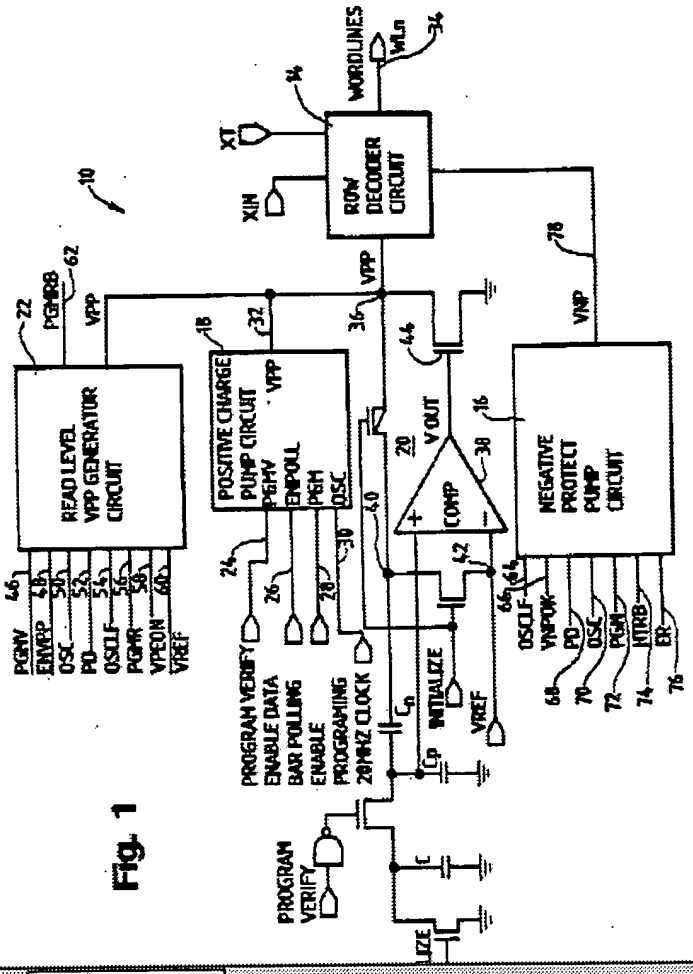

Fig. 1

US005282170A

United States Patent [19]

Van Buskirk et al.

[11] Patent Number: 5,282,170

[45] Date of Patent: Jan. 25, 1994

[54] **NEGATIVE POWER SUPPLY**

[75] Inventors: Michael A. Van Buskirk, San Jose; Jeffrey G. Hsu, Cupertino; Gang K. Chang, Sunnyvale; [illegible] B. Cleveland, Santa Clara, all of Calif.; Ashraf Mirandra, Raleigh, N.C.

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[21] Appl. No.: 964,827

[22] Filed: Oct. 22, 1992

[51] Int. Cl.[5] G11C 16/06

[52] U.S. Cl. 365/226; 363/227; 365/XXX

[58] Field of Search ..... 365/226, 227, 185, 189.01, 365/218, XXX

[56] References Cited

U.S. PATENT DOCUMENTS

5,136,480 8/1992 Kuo et al. 363/60

Primary Examiner—Terrell W. Fears
Attorney, Agent, or Firm—Davis Chin

[57] **ABSTRACT**

A negative power supply for generating and supplying a regulated negative potential to control gates of selected memory cells via wordlines in an array of flash EEPROM memory cells during flash erasure includes charge pumping means (12) formed of a plurality of charge pump stages (401-406) for generating a high negative voltage, and sensefeedback means coupled to each stage of the charge pump means for effectively cancelling out threshold voltage drops in the charge pump means. A regulator means (16) responsive to the high negative voltage and a reference potential is provided for generating the regulated negative potential so that it is independent of an external supply potential (VCC).

19 Claims, 8 Drawing Sheets